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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chih-Chin Chang
5 Appl. No.: 10/707,443 Filing Date: 12/15/2003
Examiner: Fazli Erdem Art Unit: 2826
Docket No.: LHTP0003USA

Title: LIGHT-EMITTING DIODE
10

To: Commissioner for Patents
P.O. BOX 1450
Alexandria, VA 22313-1450

15 Subject: Information disclosure statement under 37 CFR §1.56

Dear Sir,

20 This is an Information Disclosure Statement in accordance with the duty to disclose information material to patentability under 37 C.F.R. §1.56. The applicant wishes to make of record the documents listed on the accompanying form PTO/SB/08.

25 Since this IDS is filed after the mailing date of notice of allowance but before payment of the issue fee, consideration of the information disclosure statement is hereby requested according to 37 CFR §1.97(e). Each item of information contained in the information disclosure statement was first cited in an Office communication from the Taiwan Intellectual Property Office in a
30 counterpart Taiwan patent application number 92130570 on December 21, 2004,

which is not more than three months prior to the filing of the information disclosure statement.

According to the requirement set forth in 37 CFR §1.98, the applicant is submitting a copy of the cited Taiwanese patent TW 474030 (published January 21, 2002) and TW 521409 (published February 21, 2003). In accordance with MPEP 609 III A(2), an English-language equivalent application may be submitted to fulfill the requirement for a concise explanation of relevance. Accordingly, the English-language equivalent US patent 6,562,643 (issued May 13, 2003) of the Taiwanese patent TW 521409, the copies of TW 521409 and TW 474030, and English language abstract and portion (claims 1 and 2) of TW 474030 which caused it to be listed are hereby presented to fulfill the 37 CFR §1.98(a)(3) requirement.

Abstract of TW 474030 entitled
"Packaging method for light-emitting diode"

A light-emitting diode packaging method is disclosed. A substrate is preformed with a concave reflection structure. The surface of the substrate is plated with a metal conducting layer. A laser light cuts the plated metal on the surface of the concave reflection structure of the substrate to form a separate positive and negative electrode for each concave reflection structure. A light-emitting diode chip is connected with the positive and negative electrode by flip chip bonding and encapsulated by resin to yield a surface mounted type light-emitting diode. The present invention is the only one of the current surface mounted type light-emitting diode which contains both concave reflection structure and flip chip bonding, and which dissipates heat well, is small in size.

Claim 1: A light-emitting diode packaging method, in which a ceramic circuit board substrate is preformed with a concave reflection structure, the surface of the circuit board substrate is plated with a metal conducting layer, the plated metal on the surface of the concave reflection structure of the circuit board

substrate is cut by a laser light to form a separate positive and negative electrode for each concave reflection structure, and a light-emitting diode chip is connected with the positive and negative electrode by flip chip bonding and encapsulated by resin to yield a surface mounted type light-emitting diode.

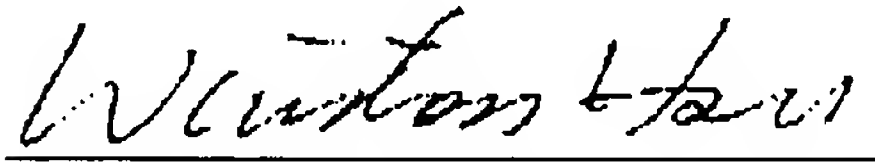
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Claim 2: The light-emitting diode packaging method of claim 1, wherein the metal conducting layer has a light reflection function and is formed of material such as silver, gold, and etc., or a structure formed by plating copper and then gold or silver.

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Respectfully submitted,

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Date: February 22, 2005

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(Use as many sheets as necessary)

Sheet	1	of	1
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Complete if Known

Application Number	10/707,443
Filing Date	12/15/2003
First Named Inventor	Chih-Chin Chang
Art Unit	2826
Examiner Name	Fazli Erdem
Attorney Docket Number	LHTP0003USA

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FOREIGN PATENT DOCUMENTS						
Examiner Initials*	Cite No. ¹	Foreign Patent Document Country Code ² Number ⁴ Kind Code ³ (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages Or Relevant Figures Appear	T ⁶
	1	TW 474030	01-21-2002			+
	2	TW 521409	02-21-2003			+

Examiner Signature		Date Considered	
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.uspto.gov or MPEP 801.04. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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